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EXAMINER	
MAGEE, THOMAS J	

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2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/072,015	Applicant(s) RUDECK ET AL.	
	Examiner Thomas J. Magee	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 13-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 13-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Cancellations

1. Applicant's cancellation of Claims 8 – 12 in Letter of March 18, 2004 is acknowledged.

Claim Objections

2. Claim 17 is objected to on the basis of being non-definitive. The phrase, "*wherein the third doping concentration has a thickness selected from a range from about 25 Angstroms to about 500 Angstroms," is* not descriptive. Examiner assumes Applicant meant to recite that the vertical phosphorous-doped oxide layer has a thickness selected from a range of about 25 Angstroms to about 500 Angstroms. Correction is required.

Claim Rejections – 35 U.S.C. 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 14 – 18 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The limitation in independent Claim 14 of "*said self align source having a resistance less than a self aligned source without the vertical phosphorous-*

doped oxide layer, thereby permitting a trench depth deeper than the self aligned source without the vertical phosphorous-doped oxide layer" is not explicitly recited in the Specivfication, and, as such, constitutes new matter.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 18 contains the phrase "such as" which renders the claim indefinite because it is unclear whether the limitations following the phrase are part of the claimed invention. See MPEP § 2173.05(d).

Claim Rejections – 35 U.S.C. 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office Action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1 – 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi et al. (US 6,657,893 B2) in view of Wu (US 6,649,308 B1) and Colabella (US 6,252,274 B1).

9. Regarding Claim 1, Takahashi et al. disclose (Col. 21, lines 10 – 50) a semiconductor device comprising a substrate (1) (Figure 1), source/drain regions (8,9,10), a first oxide layer stretching from drain to source (Col. 21, lines 51 – 54) (4), a first polysilicon layer (5)

deposited over the first oxide layer, a second oxide layer (6) deposited over the first polysilicon layer and a second polysilicon layer (7) deposited over the second oxide layer. Takahashi et al. do not disclose the presence of a self aligned source. Colabella discloses the use of the self aligned source (SAS) procedure (Col. 5, lines 22 – 44) for memory devices. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the SAS procedure of Colabella with Takahashi et al. to make leakage currents less likely to occur (Col. 4, lines 2 – 4, Colabella)
Additionally, Takahashi et al. do not disclose the presence of a phosphorous-doped oxide along the vertical edges of the gate stack. Phosphorous doped oxide spacers have been utilized in the art for about two decades. Wu discloses (Col. 4, lines 28 – 36) the presence of a phosphorous-doped oxide (16) (Figure 8) along the vertical edges of an oxide/poly/ nitride stack (Figure 8). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the phosphorous-doped oxide (PSG) spacers in Takahashi et al. to provide a dopant source for drive in to form extended source and drain regions (Col. 4, lines 60 – 65, Wu).

10. Regarding Claim 2, Takahashi et al. disclose that the first oxide layer (4) is a tunnel oxide layer (Col. 36, lines 53 – 57).

11. Regarding Claim 3, Takahashi et al. do not disclose that an oxide-nitride-oxide (ONO) layer is formed atop the first polysilicon layer as the second oxide layer, however, Colabella discloses the formation of an ONO structure atop the first polysilicon layer. It would have been obvious to one of ordinary skill in the art at the time of the invention to

combine the ONO structure of Colabella with Takahashi et al. to obtain a semiconductor device with low leakage currents and high voltage breakdown.

12. Regarding Claim 4, Takahashi et al. disclose that the first polysilicon layer (5) is a floating gate (Col. 21, lines 16 – 18).

13. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi et al. in view of Wu and Colabella, as applied to Claims 1 – 4, and further in view of Bergemont et al. (US 5,856,222).

14. Regarding Claim 5, Takahashi et al. do not explicitly disclose the presence of word-lines formed from the second polysilicon layer. Bergemont et al. disclose (Figure 5B) that the second polysilicon layer (control gate) forms a wordline.
It would have then been obvious to combine Bergemont et al.et al. with Takahashi et al., Wu, and Colabella to form an interconnected working device.

15. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Colabella in view of Wu and Rodder (US 6,329,225 B1).

16. Regarding Claim 6, Colabella discloses a semiconductor device after re-oxidation, where in the device comprises a substrate (1) (Figures 1, 2A, 3), a drain (self aligned) and source (self aligned) (8,9), a first oxide stretching from drain to source (2), a first polysilicon layer (4) over the first oxide, a second oxide (5) deposited over the first polysilicon layer, a second polysilicon layer (6) deposited over the second oxide layer, and spacers deposited along

vertical edges of the first oxide layer, the first polysilicon layer, the second oxide layer, and the second polysilicon layer.

Colabella does not disclose that the spacers consist of phosphorous-doped oxide. Wu discloses (Col. 4, lines 28 – 36) the presence of a phosphorous-doped oxide (16) (Figure 8) along the vertical edges of an oxide/poly/ nitride stack (Figure 8). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the phosphorous-doped oxide (PSG) spacers in Wu. to provide a dopant source for drive in to form extended source and drain regions (Col. 4, lines 60 – 65, Wu) in Colabella.

Colabella further does not disclose the re-oxidation profile. Rodder discloses (Col.5, lines 43 - 46) (Figure 2A) the reoxidation profile (layer 128) over the semiconductor device surface and having a height and width after formation. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Rodder with Colabella and Wu to ascertain an oxide layer profile subsequent to oxidation exposure.

17. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Colabella in view of Wu and Rodder, as applied to Claim 6, and further in view of Liu et al. (US 5,094,984) and Sobek et al. (US 6,268,624 B1).

Colabella does not disclose the structure developed at the polysilicon/oxide interfaces subsequent to reoxidation or the dependency on properties of the phosphorous-doped oxide (PSG). Sobek et al. disclose (Col. 2, lines 1 - 17) (Figure 1) that the re-oxidation process, results in inter layer encroachment and the development of "cuspate" structure characterized by a "height" and a "width." Further Sobek et al. disclose that dielectrics at the lateral edges of the

structure (Figure 3) eliminate the development of "cuspate" structure (Figure 1) characterized by a width or distance from a side edge to a vertical edge during reoxidation (Col. 4, lines 31 -36) (Abstract) and the "width" is relatively reduced compared to that without a deposited layer at the edges

As discussed above, the use of the PSG spacers disclosed by Wu will provide isolation and a diffusion source in Colabella. Liu et al. disclose that (Col. 1, line 65 through Col. 2, line 2) PSG films are porous and highly hygroscopic, depending on the phosphorous concentration. Hence, the propensity for PSG films to trap diffusing water vapor or oxygen during oxide layer growth to reduce encroachment or cuspate layer development will be dependent on the characteristics of the PSG layer.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Liu et al. and Sobek et al. with Wu, Rodder and Colabella to obtain a device with reduced or suppressed oxygen indiffusion at the edges of gate structure during re-oxidation processes.

18. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Riedel (US 6,732,241 B2) in view of Colabella, Wu and Han et al.

19. Regarding Claim 13, Riedel discloses a computer (or data processing system) (100) (Col. 3, line 56 through Col. 4, line 10) (Figure 1) comprising a processor (102), a system bus (106) and a flash memory device (114) coupled to the system bus (106). Riedel does not disclose the structure of the flash memory device. Colabella discloses the presence of a substrate (1) (Figures 1, 2A, 5), a drain (self aligned) and source (self aligned) (8,9), a first

oxide stretching from drain to source (2) , a first polysilicon layer (4) over the first oxide, a second oxide (5) deposited over the first polysilicon layer, a second polysilicon layer (6) deposited over the second oxide layer, and spacers deposited along vertical edges of the first oxide layer, the first polysilicon layer, the second oxide layer, and the second polysilicon layer.

Colabella does not disclose that the spacers formed on the vertical edges of the gate stack consist of phosphorous-doped oxide. Wu discloses (Col. 4, lines 28 – 36) the presence of a phosphorous-doped oxide (16) (Figure 8) along the vertical edges of an oxide/poly/ nitride stack (Figure 8). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the phosphorous-doped oxide (PSG) spacers in Wu. to provide a dopant source for drive in to form extended source and drain regions (Col. 4, lines 60 – 65, Wu) in Colabella.

Colabella further does not disclose the re-oxidation profile. Han et al. disclose (Figure 7) the reoxidation profile (layer 170) over the semiconductor device surface and having a height and width after formation. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Han et al. with Colabella and Wu to ascertain an oxide layer profile subsequent to oxidation exposure.

Additionally, it would have been obvious to combine Colabella, Wu, and Han et al. with Riedel to obtain a computer system with a working flash memory device.

20. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Colabella in view of Wu.

21. Regarding Claim 19, Colabella discloses a semiconductor device comprising: a substrate (1) (Figures 1, 2A, 5), a drain (self aligned) and source (self aligned) (8,9), a first oxide stretching from drain to source (2) , a first polysilicon layer (4) over the first oxide, said self aligned source extending to a point inward of an edge of the first polysilicon layer (See Figure 5), a second oxide (5) deposited over the first polysilicon layer, a second polysilicon layer (6) deposited over the second oxide layer, and spacers deposited along vertical edges of the first oxide layer, the first polysilicon layer, the second oxide layer, and the second polysilicon layer.

Colabella does not disclose that the spacers formed on the vertical edges of the gate stack consist of phosphorous-doped oxide. Wu discloses (Col. 4, lines 28 – 36) the presence of a phosphorous-doped oxide (16) (Figure 8) along the vertical edges of an oxide/poly/ nitride stack (Figure 8). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the phosphorous-doped oxide (PSG) spacers in Wu. to provide a dopant source for drive in to form extended source and drain regions (Col. 4, lines 60 – 65, Wu) in Colabella.

22. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Colabella in view of Wu, Liu et al., and Sobek et al.

23. Regarding Claim 20, Colabella discloses a semiconductor device after re-oxidation com-

prising: a substrate (1) (Figures 1, 2A, 5), a drain (self aligned) and source (self aligned) (8,9), a first oxide stretching from drain to source (2) , a first polysilicon layer (4) over the first oxide, said self aligned source extending to a point inward of an edge of the first polysilicon layer (See Figure 5), a second oxide (5) deposited over the first polysilicon layer, a second polysilicon layer (6) deposited over the second oxide layer, and spacers deposited along vertical edges of the first oxide layer, the first polysilicon layer, the second oxide layer, and the second polysilicon layer.

Colabella does not disclose that the spacers formed on the vertical edges of the gate stack consist of phosphorous-doped oxide. Wu discloses (Col. 4, lines 28 – 36) the presence of a phosphorous-doped oxide (16) (Figure 8) along the vertical edges of an oxide/poly/ nitride stack (Figure 8). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the phosphorous-doped oxide (PSG) spacers in Wu. to provide a dopant source for drive in to form extended source and drain regions (Col. 4, lines 60 – 65, Wu) in Colabella.

Additionally, Colabella does not disclose the structure developed at the polysilicon/oxide interfaces subsequent to reoxidation or the dependency on properties of the phosphorous-doped oxide (PSG). Sobek et al. disclose (Col. 2, lines 1 - 17) (Figure 1) that the re-oxidation process, results in inter layer encroachment and the development of "cuspate" structure characterized by a "height" and a "width." Further Sobek et al. disclose that dielectrics at the lateral edges of the structure (Figure 3) eliminate the development of "cuspate" structure (Figure 1) characterized by a width or distance from a side edge to a vertical edge during reoxidation (Col. 4, lines 31 -36) (Abstract) and the "width" is relatively reduced compared to

that without a deposited layer at the edges

As discussed above, the use of the PSG spacers disclosed by Wu will provide isolation and a diffusion source in Colabella. Liu et al. disclose that (Col. 1, line 65 through Col. 2, line 2) PSG films are porous and highly hygroscopic, depending on the phosphorous concentration. Hence, the propensity for PSG films to trap diffusing water vapor or oxygen during oxide layer growth to reduce encroachment or cuspate layer development will be dependent on the characteristics of the PSG layer.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Liu et al. and Sobek et al. with Wu, and Colabella to obtain a device with reduced or suppressed oxygen indiffusion at the edges of gate structure during re-oxidation processes.

Response to Arguments

24. Arguments of Applicant with respect to claim rejections have been carefully considered by Examiner, but the majority of these have been found to be unpersuasive. In regard to Claim 1, the contention that the first oxide layer (1st para., Page 10, Response) is not deposited, extending from drain to source is incorrect, as can be noted in Col. 21, lines 51 – 54. In addition, the contention of asymmetrical source/drain regions is also incorrect since mask 585 only affects region C (Figure 2) (Col. 5, lines 52 – 56). The SAS "technique" is applicable to Takahashi et al., as stated in the Office Action.

In regard to P-doped spacers, this utilization has been present in the art for almost two decades and is not novel. The reference of Wu further reads on the recitations of the instant

application. The use of LDD in EEPROM devices for suppressing gate induced drain leakage (GIDL) is also notoriously well known in the art (See Wann et al., Digest – Symp. on VLSI Tech., May 17 – 19, 1993, pp.81 –82), therefore, there is more than sufficient motivation for combining Takahashi et al. and Wu.

The commentary of Applicant in regard to Claim 6 is not germane, since Examiner is using Wu only to obtain a P-doped spacer material. As stated above, this is applicable to the primary reference. Additionally, there is no disruption in the source/drain regions, except for LDD zones, as confirmed in the prior art. There is no "teaching away" or hindsight knowledge in this instance.

Commentary on Claims 5 and 13 is moot since new bases of rejection have been presented.

Conclusions

25. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to **Thomas Magee**, whose telephone number is **(703) 305 5396.** The Examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM (EST). If attempts to reach the Examiner by telephone are unsuccessful, the examiner's supervisor, **Eddie Lee**, can be reached on **(703) 308-1690.** The fax number for the organization where this application or proceeding is assigned is **(703) 872-9306.**

Thomas Magee
June 2, 2004

Steven Loke
Primary Examiner